Regulation 2023

Program Structure

Diploma in Electronics and Communication Engineering

Program Outcomes (POs)

POs are statements that describe what students are expected to know and be able to do upon graduating from the program. These relate to the skills, knowledge, analytical ability, attitude, and behavior that students acquire through the program.

The POs essentially indicate what the students can do from subject-wise knowledge acquired by them during the program. As such, POs define the professional profile of an engineering diploma graduate.

NBA has defined the following seven POs for an Engineering diploma graduate:

PO1: Basic and Discipline-specific knowledge: Apply knowledge of basic mathematics, science and engineering fundamentals and an engineering specialization to solve the engineering problems.

PO2: Problem analysis: Identify and analyze well-defined engineering problems using codified standard methods.

PO3: Design/ development of solutions: Design solutions for well-defined technical problems and assist with the design of systems components or processes to meet specified needs.

PO4: Engineering Tools, Experimentation, and Testing: Apply modern engineering tools and appropriate technique to conduct standard tests and measurements.

PO5: Engineering practices for society, sustainability and environment: Apply appropriate technology in the context of society, sustainability, environment and ethical practices.

PO6: Project Management: Use engineering management principles individually, as a team member or as a leader to manage projects and effectively communicate about well-defined engineering activities.

PO7: Life-long learning: Ability to analyze individual needs and engage in updating in the context of technological changes.

Credit Distribution

| Semester | No of Courses | Periods | Credits |
|--------------|---------------|---------|---------|
| Semester I | 8 | 640 | 20 |
| Semester II | 9 | 640 | 20 |
| Semester III | 8 | 640 | 20 |
| Semester IV | 7 | 640 | 20 |
| Semester V | 8 | 635 | 22 |
| Semester VI | 3 | 660 | 18 |
| | Total | | 120 |

Semester III

| # | Course Category | Course Type | Code | Course Title | L-T-P | Period | Credit | End Exam |
|----|--------------------------------|-----------------------------------|------------|---|-------|--------|--------|-----------|
| 1 | Program Core | Theory | 1040233110 | Electronic Devices and Circuits | 4-0-0 | 60 | 4 | Theory |
| 2 | Program Core | Theory | 1040233210 | Digital Electronics | 4-0-0 | 60 | 4 | Theory |
| 3 | Program Core | Practical | 1040233320 | Electronic Devices and Circuits Practical | 0-0-4 | 60 | 2 | Practical |
| 4 | Program Core | Practical | 1040233420 | Digital Electronics Practical | 0-0-4 | 60 | 2 | Practical |
| 5 | Program Core | Practicum | 1040233540 | Linear Integrated Circuits | 1-0-4 | 75 | 3 | Practical |
| 6 | Engineering Science | Practicum | 1040233640 | Electrical Circuits and Machines | 1-0-2 | 45 | 2 | Practical |
| 7 | Open Elective | Advanced Skill Certification | 1040233760 | Advanced Skills Certification-3 | 2-0-2 | 60 | 2 | NA |
| 8 | Humanities & Social Science | Integrated Learning Experience | 1040233880 | Growth Lab | 0-0-3 | 45 | 0 | - |
| 9 | Audit Course | Integrated Learning Experience | 1040233981 | Induction Program–II | - | 16 | 0 | - |
| 10 | Audit Course | Integrated Learning Experience | 1040233982 | I&E/ Club Activity / Community Initiatives | - | 16 | 0 | - |
| 11 | Audit Course | Integrated Learning Experience | 1040233985 | Emerging Technology Seminars | - | 8 | 0 | - |
| 12 | Audit Course | Integrated Learning Experience | 1040233983 | Shop floor Immersion | - | 8 | 0 | - |
| 13 | Audit Course | Integrated Learning Experience | 1040233986 | Health & Wellness | 0-0-2 | 30 | 1 | NA |
| 14 | Audit Course | Integrated Learning Experience | 1040233984 | Student-Led Initiative | - | 22 | 0 | - |
| | Test & Revision | | | | | | | |
| | | Library | | | | 15 | | |
| | | Total | | | | 640 | 20 | |

Semester IV

| # | Course Category | Course Type | Code | Course Title | L-T-P | Period | Credit | End Exam |
|----|---------------------|-----------------------------------|--------------|--|-------|--------|--------|-----------|
| 1 | Program Core | Theory | 1040234110 | Microcontroller | 4-0-0 | 60 | 4 | Theory |
| 2 | Program Core | Theory | 1040234210 | Data Communication and Networking | 3-0-0 | 45 | 3 | Theory |
| 3 | Program Core | Practicum | 1040234340 | Basics of Communication Engineering | 1-0-4 | 75 | 3 | Practical |
| 4 | Program Core | Practicum | 1040234440 | Measuring Instruments and sensors | 1-0-4 | 75 | 3 | Practical |
| 5 | Engineering Science | Practicum | 1040234540 | Programming in C | 1-0-4 | 75 | 3 | Practical |
| 6 | Program Core | Project | 1040234652 | Microcontroller Practical | 0-0-4 | 60 | 2 | Project |
| 7 | Open Elective | Advanced Skill Certification | 1040234760 | Advanced Skills Certification-4 | 2-0-2 | 60 | 2 | NA |
| 9 | Audit Course | Integrated Learning Experience | 1040234882 | I&E/Club Activity/Community Initiatives | - | 30 | 0 | - |
| 10 | Audit Course | Integrated Learning Experience | 1040234887 | Special Interest groups(<i>Placement training</i>) | - | 30 | 0 | - |
| 11 | Audit Course | Integrated Learning Experience | 1040234885 | Emerging technology seminars | - | 8 | 0 | - |
| 12 | Audit Course | Integrated Learning Experience | 1040234883 | Shop Floor Immersion | - | 8 | 0 | - |
| 13 | Audit Course | Integrated Learning Experience | 1040234886 | Health & Wellness | - | 30 | 0 | - |
| 14 | Audit Course | Integrated Learning Experience | 1040234884 | Student Led Initiative | - | 24 | 0 | - |
| | | Tes | t & Revision | | | 60 | | |
| | | | Total | | | 640 | 20 | |

Semester V

| # | Course Category | Course Type | Code | Course Title | L-T-P | Period | Credit | End Exam |
|----|--------------------------------|--------------------------------------|------------|---|-------|--------|--------|-----------|
| 1 | Program Core | Practicum | 1040235130 | Advanced Communication Systems | 2-0-2 | 60 | 3 | Theory |
| 2 | Program Core | Practicum | 1040235230 | Mobile Communication | 2-0-2 | 60 | 3 | Theory |
| 3 | Program Elective | Theory | 104023531X | Elective – 1 | 3-0-0 | 45 | 3 | Theory |
| 4 | Program Core | Practicum | 1040235440 | Embedded Systems | 2-0-4 | 90 | 4 | Practical |
| 5 | Program Elective | Practicum | 104023554X | Elective – 2 | 1-0-4 | 75 | 3 | Practical |
| 6 | Open Elective | Advanced Skill Certification | 1040235660 | Advanced Skills Certification – 5 | 2-0-2 | 60 | 2 | NA |
| 7 | Humanities & Social Science | Practicum | 1040235752 | Innovation & Startup | 1-0-2 | 45 | 2 | Project |
| 8 | Project/Internship | Internship | 1040235873 | Industrial Training [Summer Vacation - 90 Hours] | - | - | 2 | Project |
| 9 | Audit Course | Integrated Learning Experience | 1040235981 | Induction program III | - | 40 | 0 | - |
| 10 | Audit Course | Integrated Learning Experience | 1040235987 | Special Interest Groups (Placement Training) | - | 40 | 0 | - |
| 11 | Audit Course | Integrated Learning Experience | 1040235986 | Health & Wellness | - | 30 | 0 | - |
| 12 | Audit Course | Integrated Learning Experience | 1040235984 | Student-Led Initiative | - | 30 | 0 | - |
| | | | | 60 | | | | |
| | | Т | otal | | | 635 | 22 | |

Elective 1

| # | Course Category | Course Type | Code | Course Title | L-T-P | Period | Credit | End Exam |
|---|------------------------|-----------------|------------------|--------------------------------------|--------------|-------------|-------------|------------|
| 1 | Program Elective | Theory | 1030235210 | E-Vehicle Technology | 3-0-0 | 45 | 3 | Theory |
| 2 | Program Elective | Theory | 1040235312 | Medical Instrumentation | 3-0-0 | 45 | 3 | Theory |
| 3 | Program Elective | Theory | 1040235313 | Digital Communication | 3-0-0 | 45 | 3 | Theory |
| 4 | Program Elective | Theory | 1040235314 | Digital Manufacturing Technology | 3-0-0 | 45 | 3 | Theory |
| 5 | Program Elective | Theory | 1040235315 | Signal & Image Processing | 3-0-0 | 45 | 3 | Theory |
| 6 | Program Elective | Theory | 1040235316 | Electronic System Design | 3-0-0 | 45 | 3 | Theory |
| 7 | Program Elective | Theory | | Inter discipline course # | 3-0-0 | 45 | 3 | Theory |
| # | Courses from other pro | grammes with th | e same credit ca | n be considered after proper approva | l from the C | Chairman, B | oard of Exa | minations. |

Elective 2

| # | Course Category | Course Type | Code | Course Title | L-T-P | Period | Credit | End Exam |
|---|------------------|-------------|------------|-----------------------------|-------|--------|--------|-----------|
| 1 | Program Elective | Practicum | 1040235541 | Industrial automation | 1-0-4 | 75 | 3 | Practical |
| 2 | Program Elective | Practicum | 1040235542 | Robotics | 1-0-4 | 75 | 3 | Practical |
| 3 | Program Elective | Practicum | 1040235543 | Computer Hardware Servicing | 1-0-4 | 75 | 3 | Practical |
| 4 | Program Elective | Practicum | 1040235544 | PCB Design & Assembly | 1-0-4 | 75 | 3 | Practical |
| 5 | Program Elective | Practicum | 1040235545 | Industrial IoT | 1-0-4 | 75 | 3 | Practical |
| 6 | Program Elective | Practicum | 1040235546 | Multimedia Systems | 1-0-4 | 75 | 3 | Practical |

| | Semester VI | | | | | | | | | | | |
|---|-------------------------|---|------------|-----------------------------|-------|--------|--------|-----------|--|--|--|--|
| # | Course Category | ory Course Type Code Course Title | | | | Period | Credit | End Exam | | | | |
| 1 | Open Elective | Theory | 600023611X | Elective-3 (Pathway) | 3-0-0 | 45 | 3 | Theory | | | | |
| 2 | Open Elective | Practicum | 104023624X | Elective-4 (Specialization) | 1-0-4 | 75 | 3 | Practical | | | | |
| 3 | Project / Internship | Project / Project / Internship Internship / Fellowship / In-house Internship Project / Industrial Training (SW) | | | | 540 | 12 | Project | | | | |
| | Total | | | | | 660 | 18 | | | | | |
| 3 | Project / Internship | Project / Internship | 1040236351 | Internship | - | 540 | 12 | Project | | | | |
| 3 | Project / Internship | Project / Internship | 1040236353 | Fellowship | - | 540 | 12 | Project | | | | |
| 3 | Project / Internship | Project / Internship | 1040236374 | In-house Project | - | 540 | 12 | Project | | | | |
| 3 | Project / Internship | Project / Internship | 2040236374 | Industrial Training (SW) | - | 540 | 12 | Project | | | | |

Elective 3 (Pathway)

| # | Course Category | Course Type | Code | Course Title | L-T-P | Period | Credit | End Exam | | | |
|--|--|-------------|------------|----------------------------------|-------|--------|--------|----------|--|--|--|
| 1 | Elective Higher Education | Theory | 6000236111 | Advanced Engineering Mathematics | 3-0-0 | 45 | 3 | Theory | | | |
| 2 | Elective Entrepreneurship | Theory | 6000236112 | Entrepreneurship | 3-0-0 | 45 | 3 | Theory | | | |
| 3 | Elective Technocrats | Theory | 6000236113 | Project Management | 3-0-0 | 45 | 3 | Theory | | | |
| 4 | Elective Technocrats | Theory | 6000236114 | Finance Fundamentals | 3-0-0 | 45 | 3 | Theory | | | |
| 5 | Elective Technologists | Theory | 1040236115 | Consumer Electronics | 3-0-0 | 45 | 3 | Theory | | | |
| 6 | Elective Technologists | Theory | 1040236116 | ASIC Design | 3-0-0 | 45 | 3 | Theory | | | |
| 7 Elective Open Elective Theory Online Elective Course \$ 3-0-0 45 3 Theory | | | | | | | | Theory | | | |
| \$ Or be c | 5 Online Courses with the same credit available in AICTE / NPTEL and reputed Institutions with proper evaluation system and certification can be considered after proper approval from the Chairman, Board of Examinations. | | | | | | | | | | |

Elective 4 (Specialization)

| # | Course Category | Course Type | Code | Course Title | L-T-P | Period | Credit | End Exam |
|---|-----------------|-------------|------------|------------------------------------|-------|--------|--------|-----------|
| 1 | Elective | Practicum | 1040236241 | Power Electronic Devices | 1-0-4 | 75 | 3 | Practical |
| 2 | Elective | Practicum | 1040236242 | VLSI Using Verilog | 1-0-4 | 75 | 3 | Practical |
| 3 | Elective | Practicum | 1040236243 | Virtual Instrumentation [Lab view] | 1-0-4 | 75 | 3 | Practical |
| 4 | Elective | Practicum | 1040236244 | Artificial Intelligence | 1-0-4 | 75 | 3 | Practical |
| 5 | Elective | Practicum | 1040236245 | Wireless Communication | 1-0-4 | 75 | 3 | Practical |
| 6 | Elective | Practicum | 1040236246 | VR and AR | 1-0-4 | 75 | 3 | Practical |

Theory

Electronic Devices and Circuits

Assessment Methodology

| | | Continuous Ass | essment (40 mark | s) | End Semester |
|-----------------------|-----------------------------|--|---|-----------------------|------------------------|
| | CA1 | CA2 | CA3 | CA4 | (60 marks) |
| Mode | Written test (Two units) | Written test (Another Two units) | Quiz MCQ (Online / Offline) | Model Examination | Written Examination |
| Duration | 2 Periods | 2 Periods | 1 Hour | 3 Hours | 3 Hours |
| Exam Marks | 50 | 50 | 60 | 100 | 100 |
| Converted to | 15 | 15 | 5 | 20 | 60 |
| Marks | 1 | 15 | 5 | 20 | 60 |
| Tentative Schedule | 6 th Week | 12 th Week | 13 th -14 th Week | 16 th Week | |

CA1 and CA2: Assessment written test should be conducted for 50 Marks for two units. The marks scored will be converted to 15 Marks. Best one out of two will be considered for the internal assessment of 15 Marks.

CA1and CA2, Assessment test should be conducted for two units as below

- PART A: (5 X 10 Marks = 50 Marks).
- Eight questions will be asked, students should write five questions. Four questions can be asked from each unit. Each question may have subdivisions. Maximum of two subdivisions shall be permitted.

CA3: 60 MCQ can be asked by covering the entire portion. It may be conducted by Online / Offline. The marks scored should be converted to 5 marks for the internal assessment.

CA4: Model examination should be conducted as per the end semester question pattern. The marks should be converted to 20 marks for the internal assessment.



DIRECTORATE OF TECHNICAL EDUCATION, CHENNAI - 600 025

| 1040233110 | Electronic Devices and | L | Т | Р | С |
|------------|------------------------|---|---|---|---|
| Theory | Circuits | 4 | 0 | 0 | 4 |

Question Pattern:

- Answer Ten questions by selecting two questions from each unit. Each question carries 10 marks.
- Four questions will be asked from every unit. Students should write any two questions. Each question may have two subdivisions only.

Question Pattern - Model Examination and End Semester Examination Theory Exam

PART- A (5 X 20 Marks = 100 Marks)

Note: Answer Ten questions by selecting two questions from each unit. Each question carries 10 marks.

Sample:

- I. 1.
 - 2.
 - 3.
 - 4.
- II. 5.
 - 6.
 - 7. 8.
- III. 9.
- 10.
- 11.
- 12. IV. 13.
- 14.
- 15.
- 16.
- V. 17.
 - 18.
 - 19.
 - 20.



| 1040223 | 110 | | 1 | т | D | C | | |
|--|--|---|---------------|--------------|---------|----|--|--|
| Theor | | Electronic Devices and | | 0 | | | | |
| Theor | У | Circuits | 4 | U | 0 | 4 | | |
| Unit I | DIOI | DE CIRCUITS | | | | | | |
| Rectifiers: Definition – Operation of Half Wave, Full Wave, and Bridge Rectifiers | | | | | | | | |
| Clippers and Clampers: Construction & Working Principle of Positive, Negative, and Biased Clippers - Construction & Working Principle of Positive and Negative Clampers | | | | | | | | |
| Opto-Electronic Devices: Definition -Symbol, Working principle, Characteristics and Applications of LED and Photo-Diode | | | | | | | | |
| Unit II | BIPC | DLAR JUNCTION TRANSISTOR | | | | | | |
| Working Principle : Construction and Working principles of NPN and PNP transistors - modes of BJT (Active, Saturation and Cut Off) | | | | | | | | |
| Transisto Biasing – I | o r Bia Fixed B | sing: Need for Biasing- Stability Factor – ⁻ Bias – Collector to Base Bias -Voltage Divider B | Type ias | es o | f | | | |
| Unit III | AMP | LIFIERS | | | | | | |
| Single St Working P Frequency | age A rincipl Respo | mplifiers: Transistor as an Amplifier and as a e of Common Emitter Amplifier- Working Princ onse characteristics of RC Coupled Amplifier | a sw ciple | itch and | - 1 | | | |
| Power A Characteri Amplifier | mplifi stics (| ers: Construction, Working Principle, Opera of Class A, Class B, Class C, and Class B p | tion oush | ano pul | t II | 12 | | |
| Multistag Configurat Constructi | e An tion on and | nplifiers: Cascade, Cascode and Darlingt (Basic concepts only) - Differential A d operation – CMRR (definition only). | con Impl | pai ifier | r : | | | |
| Unit IV | FEEC | BACK AMPLIFIERS AND OSCILLATORS | | | | | | |
| Feedback Amplifiers: Concept –Types of feedback - Positive feedback and Negative feedback- Types of negative feedback amplifiers- Effects of Negative feedback | | | | | | | | |
| Theory of (Barkhaus | f Osci l en Cri | llation: Tank Circuit-Conditions for Oscillation terion) - Classifications | | | | 12 | | |
| Oscillator Hartley Os Shift Oscil | r Circ u scillato lator a | uits : Construction, Working Principle and Ope r, Colpitts Oscillator, Wien bridge Oscillator, F nd Crystal Oscillator | ratio RC P | on o hase | f | | | |
| | DIREC | TORATE OF TECHNICAL EDUCATION, CHENNAI – (| 600 0 | 25 | | | | |



| 1040233110Electronic Devices and Circuits | | L | Т | Р | С | |
|--|--|-------------|---|---|---|----|
| | | Circuits | 4 | 0 | 0 | 4 |
| Unit V FIELD EFFECT TRANSISTORS & UNI JUNCTION TRANSISTOR | | | | | | |
| FET: Definition and Types - Comparison between FET and BJT- Construction and Working principle of N Channel JFET- Drain and Transfer Characteristics of JFET. | | | | | | |
| MOSFET (N Channel Enhancement and Depletion Mode): Construction, Working Principle, Operation and Characteristics. | | | | | | 12 |
| UJT: Construction-Equivalent circuit -Operation-Characteristics- UJT as a Relaxation Oscillator. | | | | | s | |
| | | TOTAL HOURS | | | | 50 |

Suggested List of Students Activity

- Presentation/Seminars by students on any recent technological developments based on the course.
- Periodic class quizzes conducted on a weekly/fortnightly based on the course.
- Mini project that shall be an extension of any practical lab exercise to real-world application.

Text Books

- 1. R.S.Sedha, A Textbook of Applied Electronics, 3rd edition, S.Chand Publications, 2012
- Thomas L. Floyd, Electronic Device, 10th edition, Pearson Education, 2018
- Boylestad&Nashlesky, Electronic Devices and Circuit Theory, 10th edition, PHI, 2009

Suggested links for Students activities

- <u>https://www.tinkercad.com/</u>
- <u>https://www.multisim.com/</u>



| 1040233110 | Electronic Devices and | L | Т | Ρ | С |
|------------|------------------------|---|---|---|---|
| Theory | Circuits | 4 | 0 | 0 | 4 |

Web-based/Online Resources

- <u>https://onlinecourses.nptel.ac.in/noc21_ee80/preview</u>
- <u>https://learn.sparkfun.com/</u>
- <u>https://www.allaboutcircuits.com/textbook/digital/</u>
- http://electronicstheory.com/COURSES/ELECTRONICS/e101-1.htm
- <u>https://www.gadgetronicx.com/electronic-circuits-library/</u>



Theory

Introduction

Digital Electronics is the Branch of Electronics that deals with the representation and manipulation of data in digital form. Digital systems have become an integral part of our daily lives, and there are countless examples of their applications in various fields. The main objective of this course is to introduce and provide basic idea about binary number system, digital logic gates, arithmetic operations, combinational and sequential logics and memory devices.

Course Objectives

The objective of this course is to enable the student to

- Familiarize with the different number systems and binary operations
- Build simple logic circuits using basic gates and able to simplify Boolean functions
- Know and design simple combinational logics using basic gates and to optimize Boolean logic using Karnaugh maps.
- Understand the basic sequential logic components: SR Latch, D Flip-Flop and their usage and make the students able to understand the sequential logic circuits.

Course Outcomes

On successful completion of this course, the student will be able to

- CO1: Understand different number systems and their conversion from one to others, codes used in digital computers and communication systems.
- CO2: Know the positive and negative logic, logic gates, logical Variables, Truth Table and construction of logic circuits using logic gates.
- CO3. Learn the basic properties of Boolean algebra and minimize the Boolean Functions using Boolean laws and K–Map to construct circuits.
- CO4: Understand the working mechanism of different Combinational, Sequential circuits and their role in the digital system design.
- CO5: Know the technology and organization of different memory devices used in digital circuits for real world application.

Pre-requisites

Knowledge of Basic Science



DIRECTORATE OF TECHNICAL EDUCATION, CHENNAI - 600 025

Theory

Assessment Methodology

| | (| End Semester | | | |
|-----------------------|-----------------------------|--|---|-----------------------|------------------------|
| | CA1 | CA2 | CA3 | CA4 | (60 marks) |
| Mode | Written test (Two units) | Written test (Another Two units) | Quiz MCQ (Online / Offline) | Model Examination | Written Examination |
| Duration | 2 Periods | 2 Periods | 1 Hour | 3 Hours | 3 Hours |
| Exam Marks | 50 | 50 | 60 | 100 | 100 |
| Converted to | 15 | 15 | 5 | 20 | 60 |
| Marks | 1 | 15 | 5 | 20 | 60 |
| Tentative Schedule | 6 th Week | 12 th Week | 13 th -14 th Week | 16 th Week | |

CA1 and CA2: Assessment written test should be conducted for 50 Marks for two units. The marks scored will be converted to 15 Marks. Best one out of two will be considered for the internal assessment of 15 Marks.

CA1and CA2, Assessment test should be conducted for two units as below

- PART A: (5 X 10 Marks = 50 Marks).
- Eight questions will be asked, students should write Five questions. Four questions can be asked from each unit. Each question may have subdivisions. Maximum of two subdivisions shall be permitted.

CA3: 60 MCQ can be asked by covering the entire portion. It may be conducted by Online / Offline. The marks scored should be converted to 5 marks for the internal assessment.

CA4: Model examination should be conducted as per the end semester question pattern. The marks should be converted to 20 marks for the internal assessment.



DIRECTORATE OF TECHNICAL EDUCATION, CHENNAI - 600 025

2023 REGULATION

Digital Electronics

L T P C 4 0 0 4

Theory

Question Pattern:

- Answer Ten questions by selecting two questions from each unit. Each question carries 10 marks.
- Four questions will be asked from every unit. Students should write any two questions. Each question may have two subdivisions only.

Question Pattern - Model Examination and End Semester Examination Theory Exam

PART- A (5 X 20 Marks = 100 Marks) Note: Answer Ten questions by selecting two questions from each unit. Each question carries 10 marks.

Sample:

- I. 1.
 - 2.
 - 2. 3.
 - 3. 4.
- II. 5.
- 7.
- 8.
- III. 9.
 - 10.
 - 11.
- 12. IV. 13.
 - 14.
 - 15.
 - 16.
- V. 17.
 - 18.
 - 19.
 - 20.



| 1040233 | 210 | | L | Т | Ρ | С |
|--|------|--------------------------------|---|---|------------------|----|
| Theor | У | Digital Electronics | | 0 | 0 | 4 |
| Unit I | NUM | BER SYSTEM AND BOOLEAN ALGEBRA | | | | |
| Number system and Codes: Decimal, Binary, Octal and Hexa Decimal – conversion between the number systems – 1's and 2's Complement - Binary addition and subtraction - Special Codes: BCD, ASCII code, Gray code Boolean Algebra: Basic Boolean laws – Demorgan's Theorems – SOP and POS representation– Karnaugh Map: Simplification of Boolean expression using K-Map (up to 4 variables in SOP form) | | | | | a 5 7 7 | 12 |
| Unit II | LOG | C GATES & CIRCUIT REALIZATION | | | | |
| Logic Gates: Symbol, Logical Expression, and Truth Table for AND, OR, NOT, NAND, NOR, Ex-OR and Ex-NOR gates - Universal Gates: NAND and NOR. Logic Circuit Realization: Realization of logic gates using Universal gates - Implementation of Boolean expression using Logic Gates | | | | | ': 1 | 2 |
| Unit III | СОМ | BINATIONAL LOGIC CIRCUITS | | | | |
| Arithmetic Circuits: Half Adder, Full Adder, Half Subtractor, Full Subtractor: Operation, Truth table, Logical expression, and diagram. Data Processing Circuits: Operation, Truth table, Logical expression, and diagram of Encoder (4 to 2 and 8 to 3) - Decoder (2 to 4 and 3 to 8) - Multiplexer (4 to 1) -Demultiplexer (1 to 4) - Parity generator and enables (2 bits) | | | | | ,) 1 | 12 |
| Unit IV | SEQU | IENTIAL LOGIC CIRCUITS | | | • | |
| Flip Flops – Basic Latches using NAND and NOR gates –Triggering: Types of Triggering (Definitions only) – Logic diagram, Truth table and operation of Clocked SR Flip-Flop using NAND gates –Preset and Clear (Need and Concept only) – Logic diagram, Truth table and Operation of D, JK, T Flip-Flop and Master Slave Flip-Flop – Applications of Flip-Flops Counters: Definition and types - Difference between Synchronous and Asynchronous Counters – Logic diagram, truth table and operation of 4-bit Asynchronous and Synchronous Counters - Decade Counter – Applications of Counter | | | | | | 12 |



| 1040233210 Theory | | | | | | | |
|---|--|---------------------|---|---|---|----|--|
| | | Digital Electronics | 4 | 0 | 0 | 4 | |
| Unit V SHIFT REGISTERS AND STORAGE DEVICES | | | | | | | |
| Shift Registers: Definition – Logic diagram and Operation of Serial in Serial out, Parallel in Serial Out, Serial in Parallel Out and Parallel in Parallel Out – Applications of Registers Memory: ROM – types of ROM (PROM, EPROM, EEPROM and Flash (Simple description only) – RAM: Simple structure of SRAM and DRAMs – Comparison between RAM and ROM – comparison between SRAM and DRAM-Principles of Cache memory and associative memory (Basic | | | | | | 12 | |
| TOTAL HOURS | | | | | | 50 | |

Suggested List of Students Activity

- Presentation/Seminars by students on any recent technological developments based on the course.
- Periodic class quizzes conducted on a weekly/fortnightly based on the course.
- Mini project that shall be an extension of any practical lab exercise to real-world application.



Digital Electronics

| L | Т | Ρ | С |
|---|---|---|---|
| 4 | 0 | 0 | 4 |

Theory

Text Books

- 1. Thomas L. Floyd, Digital Fundamentals, 11th edition, Pearson Education, 2017
- 2. S. Salivahanan and S. Arivazhagan, Digital Circuits and Design, 5th edition, Vikas Publishing House Pvt. Ltd, 2019
- 3. Anil K. Maini, Digital Electronics principles and integrated circuits, 1st edition, Wiley Publications, 2007

Web-based/Online Resources

- https://www.electronics-tutorials.ws/
- https://learn.sparkfun.com/
- https://www.allaboutcircuits.com/textbook/digital/
- http://electronicstheory.com/COURSES/ELECTRONICS/e101-1.htm
- https://www.gadgetronicx.com/electronic-circuits-library/
- https://www.electronics-lab.com/
- https://learn.adafruit.com/
- https://www.instructables.com/circuits/
- https://www.digitalelectronicsdeeds.com/
- https://www.electrical4u.com/digital-electronics/
- https://www.tutorialspoint.com/digital circuits/index.htm



Practical

| L | Т | Ρ | С |
|---|---|---|---|
| 0 | 0 | 4 | 2 |

Introduction

Every Electronics Engineer should have knowledge about the components used in Electronics. By doing practical experiments in this course, they will be skilled in handling electronic circuits and able to apply the skill in Electronic Systems.

Course Objectives

The objective of this course is to

- Familiarize with basic Electronic Devices PN Junction Diode, Zener Diode, BJT and UJT.
- Understand the working of FET and MOSFET.
- Know the working of Clippers and Clampers.
- Acquire knowledge on RC coupled Amplifier, RC Phase Shift Oscillator.
- Understand the working of Astable Multivibrator

Course Outcomes

After successful completion of this course, the students should be able to

- CO1: Test the working of PN Junction Diode, Zener Diode.
- CO2: Test the working of BJT, UJT and FET.
- CO3: Test the working of Clippers and Clampers.
- CO4: Check the performance of RC Coupled Amplifier, RC phase shift Oscillator.
- CO5: Test the working of Astable Multivibrator.

Pre-requisites

Knowledge on Electronic Devices and Circuits



Practical

| L | Т | Ρ | С |
|---|---|---|---|
| 0 | 0 | 4 | 2 |

Instructional Strategy

• Practice approach may be followed throughout the course so that students are able to understand and grasp the concepts and principles.

Assessment Methodology

| | C | End Semester | | | |
|-----------------------|------------------------------------|--|-----------------------|-----------------------|--------------------------|
| | CA1 | CA2 | CA3 | CA4 | (60 marks) |
| Mode | Practical Test | Practical Test | Practical Document | Practical Test | Practical Examination |
| Portion | First Cycle / 50 % Exercises | Second Cycle / Another 50 % Exercises | All Exercises | All Exercises | All Exercises |
| Duration | 2 Periods | 2 Periods | Regularly | 3 Hours | 3 Hours |
| Exam Marks | 50 | 50 | 100 | 100 | 100 |
| Converted to | 10 | 10 | 10 | 20 | 60 |
| Marks | - | 10 | 10 | 20 | 60 |
| Tentative Schedule | 7 th Week | 14 th Week | 15 th Week | 16 th Week | |

Note:

CA1 and CA2: All the exercises/experiments as per the portions mentioned above should be completed and kept for the practical test. The students shall be permitted to select any one by lot for the test. The practical test should be conducted per the scheme of evaluation as below. The marks awarded will be converted to 10 Marks for each assessment test. The best one out of two will be considered for the internal assessment of 10 Marks.



DIRECTORATE OF TECHNICAL EDUCATION, CHENNAI - 600 025

Practical

SCHEME OF EVALUATION

| Part | Description | Marks |
|------|--|-------|
| А | Aim | 5 |
| В | Circuit Diagram & Tabular Column | 20 |
| С | Connection/Procedure, Observation/Reading Taken & Calculations | 20 |
| D | Result/Output | 5 |
| | 50 | |

CA 3: Practical document should be maintained for every exercise immediately after completion of the practice. The same should be evaluated for 10 Marks. The total marks awarded should be converted to 10 Marks for the internal assessment. The practical document should be submitted for the Practical Test and End Semester Examination with a bonafide certificate

The details of the documents to be prepared as per the instruction below

- The exercise should be completed on the day of practice.
- The same shall be evaluated for 10 marks on the day or next day of practice before commencement of the next exercise.
- This documentation can be carried out in a separate notebook / file. The procedure and sketch should be written by the student manually.
- The detailed date of the practices and its evaluations should be maintained in the course logbook. The log book and the practical documents should be submitted for the verification by the Flying Squad and DOTE Official.

CA 4: All the exercises should be completed and kept for the practical test. The students shall be permitted to select any one by lot for the test. The practical test should be conducted as per the scheme of evaluation as below. The marks awarded should be converted to 20 Marks for the internal assessment.



DIRECTORATE OF TECHNICAL EDUCATION, CHENNAI - 600 025

Practical

| L | Т | Ρ | С |
|---|---|---|---|
| 0 | 0 | 4 | 2 |

SCHEME OF EVALUATION

| Part | Description | Marks |
|------|--|-------|
| A | Aim | 5 |
| В | Circuit Diagram | 25 |
| С | Tabular Column& Model Graph | 10 |
| D | Connection/Procedure, Observation/Reading Taken & Calculations | 30 |
| E | Result/Output | 20 |
| F | Viva Voce | 10 |
| | 100 | |



| 1040233320 | | Electronic Devices and | L | Т | Ρ | С |
|--|--|--|-------------|-------------|----|------------|
| Practical | | Circuits Practical | 0 | 0 | 4 | 2 |
| Ex.No | | Name of the Experiment | | | Но | urs |
| 1 Test a PN Junction diode and construct a circuit using it to 1 verify the Forward and Reverse Bias Characteristics. Find the value of its cut-in voltage | | | | | | 3 |
| 2 | Test a the Fo value o | Zener Diode and construct a circuit using it t prward and Reverse Bias Characteristics. Fi of its Reverse Breakdown Voltage. | o ve ind | rify the | | 3 |
| 3 | Constr output | uct a Half Wave Rectifier and Test its inp waveforms. | out a | and | | 3 |
| 4 | Constr and ou | uct a Full Wave (Bridge) Rectifier and Test it ant test it at the set it at the set of t | s in | put | | 3 |
| 5 | Constr input a | uct a Common Emitter Transistor Circuit and and Output Characteristic curves. | Test | its | | 3 |
| 6 | Constr input a | uct a Common Base Transistor circuit and and output Characteristic curves. | test | its | | 3 |
| 7 | 7 Construct a Common Source Field Effect Transistor circuit and test its Characteristic curves. | | | | | 3 |
| 8 Construct a circuit and test the Negative Resistance Characteristics of UIT. | | | | | | 3 |
| 9 | Constr Negati | uct and test the working of Positive Clipp ve Clipper. | er a | and | | 3 |
| 10 Construct and test the working of positive clamper and Negative Clamper. | | | | | | 3 |
| 11 Using open source Software tool, find the Frequency response of RC coupled amplifier. | | | | | 3 | |
| 12 | Test t softwa | he working of Colpitts circuit using open re tool. | sou | rce | | 3 |
| 13 Test the working of Astable Multivibrator using open source software tool. | | | | | | 3 |
| 14 | Test tl softwa | he working of Hartley oscillator using open re tool. | sou | rce | | 3 |
| 15Test the working of RC Phase Shift Oscillator using open source Software Tool. | | | | | | 3 |
| | | Revision | | | 1 | .5 |
| | | TOTAL HOURS | | | 6 | i 0 |



Practical

| L | Т | Ρ | С |
|---|---|---|---|
| 0 | 0 | 4 | 2 |

Suggested Activity

Apart from laboratory learning, Teachers should use the following strategies to achieve the various outcomes of the course.

- Different methods of teaching and media to be used to attain attention.
- Micro-projects may be given to group of students for hand-on experiences.

Reference Books

- 1. S.Salivahanan, N. Suresh Kumar and A.Vallavaraj, Electronic Devices& Circuits, 3rd edition, Tata McGraw Publication,2016
- 2. BoylestadandNashlesky, Electronic Devices and Circuit Theory, $10^{\rm th}$ edition, PHI, 2009
- 3. Albert Malvinoand David J. Bates, Electronic Principles, 7th edition, Tata McGraw Hill Publication, 2017

| S.No | Name of the Equipments | Range | Required Nos. |
|------|---------------------------------|--------------|------------------|
| 1 | DC Regulated power supply | 0-30V,1A | 10 |
| 2 | Signal Generator | 1MHz | 4 |
| 3 | Dual trace CRO | 20MHz/ 30MHz | 5 |
| 4 | Digital Multimeter | - | 10 |
| 5 | DC Voltmeter (Analog/Digital) | - | 10 |
| 6 | DC Ammeter (Analog/Digital) | - | 15 |
| 7 | Open source software : Multisim | - | - |

List of Equipments





| L | Т | Ρ | С |
|---|---|---|---|
| C | 0 | 4 | 2 |

Practical

Assessment Methodology

| | C | ontinuous Assess | ment (40 mark | s) | End Semester | | |
|-----------------------|------------------------------------|--|-----------------------|-----------------------|--------------------------|--|--|
| | CA1 | CA2 | CA3 | CA4 | (60 marks) | | |
| Mode | Practical Test | Practical Test | Practical Document | Practical Test | Practical Examination | | |
| Portion | First Cycle / 50 % Exercises | Second Cycle / Another 50 % Exercises | All Exercises | All Exercises | All Exercises | | |
| Duration | 2 Periods | 2 Periods | Regularly | 3 Hours | 3 Hours | | |
| Exam Marks | 50 | 50 | 100 | 100 | 100 | | |
| Converted to | 10 | 10 | 10 | 20 | 60 | | |
| Marks | - | 10 | 10 | 20 | 60 | | |
| Tentative Schedule | 7 th Week | 14 th Week | 15 th Week | 16 th Week | | | |

Note:

CA1 and CA2: All the exercises/experiments as per the portions mentioned above should be completed and kept for the practical test. The students shall be permitted to select any one by lot for the test. The practical test should be conducted per the scheme of evaluation as below. The marks awarded will be converted to 10 Marks for each assessment test. The best one out of two will be considered for the internal assessment of 10 Marks.

SCHEME OF EVALUATION

| Part | Description | Marks |
|------|--|-------|
| А | Aim | 5 |
| В | Circuit Diagram & Tabular Column | 20 |
| С | Connection/Procedure, Observation/Reading Taken & Calculations | 20 |
| D | Result/Output | 5 |
| | 50 | |



DIRECTORATE OF TECHNICAL EDUCATION, CHENNAI – 600 025

| L | Т | Ρ | С |
|---|---|---|---|
| 0 | 0 | 4 | 2 |

Practical

CA 3: Practical document should be maintained for every exercise immediately after completion of the practice. The same should be evaluated for 10 Marks. The total marks awarded should be converted to 10 Marks for the internal assessment. The practical document should be submitted for the Practical Test and End Semester Examination with a bonafide certificate

The details of the documents to be prepared as per the instruction below

- The exercise should be completed on the day of practice.
- The same shall be evaluated for 10 marks on the day or next day of practice before commencement of the next exercise.
- This documentation can be carried out in a separate notebook / file. The procedure and sketch should be written by the student manually.
- The detailed date of the practices and its evaluations should be maintained in the course logbook. The log book and the practical documents should be submitted for the verification by the Flying Squad and DOTE Official.

CA 4: All the exercises should be completed and kept for the practical test. The students shall be permitted to select any one by lot for the test. The practical test should be conducted per the scheme of evaluation as below. The marks awarded should be converted to 20 Marks for the internal assessment.

| SCHEME O | F EVALUATION |
|----------|--------------|
|----------|--------------|

| Part | Description | Marks | | | |
|------|--|-------|--|--|--|
| А | Aim | 5 | | | |
| В | Circuit Diagram | 30 | | | |
| С | Truth Table | 15 | | | |
| D | Connection/Procedure, Observation/Reading Taken & Calculations | 20 | | | |
| E | Result/Output | 20 | | | |
| F | Viva Voce | 10 | | | |
| | TOTAL MARKS 100 | | | | |



| 1040233420 Practical | | Digital Electronica Drastical | aital Electronics Practical | | | С |
|--|---|---|-----------------------------|-----|----|-----|
| | | Digital Electronics Practical | 0 | 0 | 4 | 2 |
| Ex.No | | Name of the Experiment | | | Но | urs |
| 1 | Verifica EX-OR | ation of truth table of OR, AND, NOT, NOR, gates. | NAI | ND, | | 3 |
| 2 | Realiza | ation of Logic Gates using NAND gates. | | | | 3 |
| 3 | Verifica | ation of Demorgan's theorems. | | | | 3 |
| 4 | Full ad | der using Logic Gates. | | | , | 3 |
| 5 | Full Su | btractor using Logic Gates. | | | , | 3 |
| 6 | Constr | uction and Verification of Truth Table for Multip | olexe | er. | | 3 |
| 7 | Constr multip | uction and Verification of truth table following | or I | De- | | 3 |
| 8 | Construction and Verification of truth table one digit digital comparator. | | | | | |
| 9 | Construction and Verification of truth table for SR Latch using NAND gates. | | | | | |
| 10 | Construct and test the performance of Parity Generator. | | | | | 3 |
| 11 | Construction and verification of Truth Table for JK and T Flip-Flops. | | | | | 3 |
| 12 | Construct and test the performance of a 4-bit Asynchronous up counter. | | | | | 3 |
| 13 | Construct and test the performance of a Decade Counter. | | | | | 3 |
| 14 | Construct and test Shift Register in SIPO using D flip-flops. | | | | | 3 |
| 15 Construct and test Shift Register in PISO using D flip-flops. | | | | | | 3 |
| | Revision | | | | | |
| | | TOTAL HOURS | | | 6 | 50 |



DIRECTORATE OF TECHNICAL EDUCATION, CHENNAI – 600 025

Linear Integrated Circuits

Practicum

Assessment Methodology

| | C | ontinuous Asses | ssment (40 mark | s) | End Semester | | |
|-----------------------|---|--|------------------------|-----------------------|--------------------------|--|--|
| | CA1 | CA2 | CA3 | CA4 | (60 marks) | | |
| Mode | Practical Test | Practical Test | Written Test Theory | Practical Test | Practical Examination | | |
| Portion | Cycle I Experiments/ 50% Experiments | Cycle II Experiments/ Another 50% Experiments | All Units | All Experiments | All Experiments | | |
| Duration | 2 Periods | 2 Periods | 3 hours | 3 hours | 3 hours | | |
| Exam Marks | 60 | 60 | 100 | 100 | 100 | | |
| Converted to | 10 | 10 | 15 | 15 | 60 | | |
| Marks | 1 | 0 | 15 | 15 | 60 | | |
| Tentative Schedule | 7 th Week | 14 th Week | 15 th Week | 16 th Week | | | |

Note:

CA1 and CA2: All the exercises/experiments should be completed as per the portions above and kept for the practical test. The students shall be permitted to select any one by lot for the test. The practical test should be conducted as per the scheme of evaluation as below. The marks awarded shall be converted to 10 Marks for each assessment test. The best one out of two will be considered for the internal assessment of 10 Marks.

Practical documents should be maintained for every experiment immediately after completion of the practice. The practical document should be submitted for the practical test. The same should be evaluated for 10 Marks for each exercise/experiment. The total marks awarded should be converted to 10 Marks for the practical test as per the scheme of evaluation as below.



DIRECTORATE OF TECHNICAL EDUCATION, CHENNAI - 600 025

Practicum

The details of the documents to be prepared as per the instruction below

- The experiment should be completed on the day of practice.
- The same shall be evaluated for 10 marks on the day or next day of practice before commencement of the next experiment.
- This documentation can be carried out in a separate notebook / printed manual / file. The Circuit Diagram, Readings, Calculations and Graph/Result should be written by the student manually.
- The detailed date of the practices and its evaluations should be maintained in the course logbook. The log book and the practical documents should be submitted for the verification by the Flying Squad and DOTE Official.

SCHEME OF EVALUATION

| Part | Description | Marks |
|------|-------------------------------------|-------|
| А | Aim | 5 |
| В | Circuit Diagram | 20 |
| С | Connections / Output | 25 |
| D | Practical document (All Practicals) | 10 |
| | 60 | |

CA 3: Written Test for complete theory portions should be conducted for 100 Marks as per the question pattern below. The marks scored will be converted to 15 Marks for internal assessment.

Question pattern – Written Test Theory

| | Description | Marks | | |
|----------|--------------------------------|-----------------------|---|--|
| Part – A | 30 MCQ Questions. | 30 X 1 Mark | 30 Marks | |
| Part – B | 7 Questions to be answered out | 7 X 10 Marks | 70 Marks | |
| | of 10 Questions. | , <u>, , 10 Harks</u> | , | |



| 1040233540 | Linoar Integrated Circuite | L | Т | Ρ | С |
|------------|----------------------------|---|---|---|---|
| Practicum | Linear Integrated Circuits | 1 | 0 | 4 | 3 |

CA 4: All the exercises/experiments should be completed and kept for the practical test. The students shall be permitted to select any one by lot for the test. The practical test should be conducted as per the scheme of evaluation below. After completion of all the exercises the practical test should be conducted as per End Semester Examination question pattern scheme of evaluation. The marks awarded should be converted to 15 Marks for the internal assessment.

SCHEME OF EVALUATION

Model Practical Examination and End Semester Examination - Practical Exam

| Part | Description | Marks |
|------|-------------------------|-------|
| А | Aim | 5 |
| В | Circuit Diagram | 20 |
| С | Connections / Execution | 25 |
| D | Output / Result | 10 |
| E | Written Test | 30 |
| F | Viva Voce | 10 |
| | 100 | |

Note: For the written test 30 MCQ shall be asked from the theory portions.



| 10402 | 3354 | 10 | Linear Integrated Circuite | L | Т | Ρ | С |
|--|--|---|--|---------------|-----------|---|-----|
| Pract | ticum | | | 1 | 0 | 4 | 3 |
| Unit I | Ι | NT | RODUCTION TO OPERATIONAL AMPLIFIER | s | | | |
| Integrated Circuit- Classification of IC- Operational Amplifier IC 741- Schematic symbol for Op-Amp-pin diagram of IC 741-Block diagram of an Op-Amp, Characteristics of an ideal Op-Amp, CMRR, Slew Rate- Basic Linear Circuits-Inverting Amplifier, Non-Inverting Amplifier (Qualitative treatment only) | | | | | | 3 | |
| Ex.No | | | Name of the Experiment | | | | |
| 1 2 | Test the performance of Inverting Amplifier with waveforms for input and output signals.Test the performance of Non-Inverting Amplifier with waveforme for input and output signals. | | | | - 6 | 5 | |
| Unit I | OPAMP APPLICATIONS | | | | | | |
| Summing amplifier-Multiplier-Divider-Voltage follower-Comparator-zero crossing detector-Integrator-Differentiator. | | | | | | 3 | |
| Ex.No | Name of the Experiment | | | | | | |
| 3 | Test IC74 | tł 1. | e performance of Summing amplifierusing | Op- | Amp | | |
| 4 | Test | the | e performance of Voltage followerusing Op-Amp | IC7 | 41. | | 1 - |
| 5 | Test IC74 | th 1. | e performance of Zero crossing detectorusing | Op- | Amp | | 12 |
| 6 | Test | the | e performance of Integratorusing Op-Amp IC741 | L. | | | |
| 7 | Test | the | e performance of Differentiatorusing Op-Amp IC | 741. | | | |
| Unit III WAVEFORM GENERATORS AND PLL | | | | | | | |
| Wavefo Tooth V | orm g Nave | ene Ge | erators-Square wave, Triangular wave, Sine wa nerators.Phase Locked Loops -Basic principles o | ave, f PLI | Saw L. | | 3 |
| Ex.No | | | Name of the Experiment | | | | |
| 8 | Gene | era | te Square wave using Op-Amp IC741. | | | | 6 |
| 9 | Gene | enerate Triangular wave using Op-Amp IC741. | | | | | σ |



| 10402 | 33540 | | L | Т | Ρ | С |
|---|---|--|----------|------|---|----|
| Practicum | | Linear Integrated Circuits | 1 | 0 | 4 | 3 |
| Unit I | / D// | A AND A/D CONVERTERS | | | | |
| D/A conver | CONVEI sion-We | RTERS: Digital to Analog converter-Basics ighted Resistor D/A Converter – R-2R Ladder D/ | of A. | D/A | | 2 |
| A/D CONVERTERS: Analog to Digital Converter-Basics of A/D conversion-Types of A/D converter-Block diagram of Flash type ADC,Successive approximation ADC. | | | | | | 2 |
| Ex.No | | Name of the Experiment | | | | |
| 10 | Design using (| and implement the Binary Weighted Resistor Dp-Amp IC741. | DA | C by | | 6 |
| 11 | Design and implement the R-2R Ladder DAC by using Op-Amp IC741. | | | | | - |
| Unit V | SPI | ECIAL FUNCTION ICs | | | | |
| IC 555 Timer – Pin diagram of IC 555 -Functional Block diagram of IC555-Applications-AstableMultivibrator-Mono stable Multivibrator-Schmitt trigger. IC voltage regulators-Linear fixed voltage regulator-Positive voltage regulator using IC 78XX, negative voltage regulator using IC 79XX-LDO regulators. | | | | | | 3 |
| Ex.No | | Name of the Experiment | | | | |
| 12 | Test th Timer. | ne performance of Astable Multivibrator using | IC | 555 | | |
| 13 | Test the performance of Mono stable Multivibrator using IC 555 Timer. | | | | | |
| 14 | Test the performance of Schmitt trigger using IC 555Timer.12 | | | | | |
| 15 | Test the line regulation for anyone positive voltage regulator using IC 78xx and anyone negative voltage regulator using IC 79xx. | | | | | |
| | REVISION | | | | | 15 |
| | | TOTAL HOURS | | | | 75 |



Practicum

Suggested List of Students Activity

- Presentation/Seminars by students on any recent technological developments based on the course.
- Periodic class quizzes conducted on a weekly/fortnightly based on the course
- Micro project that shall be an extension of any practical lab exercise to real-world application

Text Books

- 1. D. Roy Choudhry and Shail Bala Jain, Linear Integrated Circuits, 6th edition, New Age International Pvt.Ltd., 2021
- 2. Sergio Franco, Design with Operational Amplifiers and Analog Integrated Circuits, 3rd edition, Tata McGrawHill, 2017
- 3. S. Salivahanan and V.S. Kanchana Bhaskaran, Linear Integrated Circuits, 1st edition, Tata McGraw Hill, 2018

List of Equipments required for a Batchof 30 students

| SI.No | Equipments | Quantity |
|-------|-----------------------------|----------|
| 1 | Dual Regulated Power supply | 6 |
| 2 | CRO/DSO | 6 |
| 3 | Function Generator | 6 |



| L | Т | Ρ | С |
|---|---|---|---|
| 1 | 0 | 2 | 2 |

Practicum

Introduction

This course will provide an outline of Electrical Circuits and Machines that are relevant to the ECE branch.

Course Objectives

On successful completion of the course, the students must be able to

- Understand the fundamentals of DC circuits.
- Know the basic concepts of Network theorems.
- Know the basic concepts of AC circuit behavior.
- Understand resonance in series and parallel circuits.
- Know the operation of the Transformer.
- Know the operation of different Electrical machines.

Course Outcomes

After successful completion of this course, the students should be able to

- CO1: Reduce the complex circuits using Reduction Techniques.
- CO2: Apply Network Theorems in DC Circuits.
- CO3: Analyze AC circuits.
- CO4: Analyze AC series and parallel resonance networks.
- CO5: Understand the working principle and Applications of Electrical Machines.

Pre-requisites

Knowledge about basic electronic concepts and Laws



Practicum

Electrical Circuits and Machines

| L | Т | Ρ | С |
|---|---|---|---|
| 1 | 0 | 2 | 2 |

CO/PO Mapping

| CO / PO | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 | P07 |
|---------|-----|-----|-----|-----|-----|-----|-----|
| CO1 | 3 | 3 | 3 | 3 | - | - | 3 |
| CO2 | 3 | 2 | 3 | 3 | - | - | 3 |
| CO3 | 3 | 2 | 3 | 3 | - | - | 3 |
| CO4 | 3 | 2 | 3 | 3 | - | - | 3 |
| CO5 | 3 | 2 | 3 | 3 | - | - | 3 |

Legend: 3-High Correlation, 2-Medium Correlation, 1-Low Correlation

Instructional Strategy

- It is advised that teachers take steps to pique pupils' attention and boost their learning confidence.
- To help students learn and appreciate numerous concepts and principles in each area, teachers should provide examples from daily life, realistic situations, and real-world engineering and technological applications.
- The demonstration can make the subject exciting and foster in the students a scientific mindset. Student activities should be planned on all the topics.
- Throughout the course, a theory-demonstrate-practice-activity strategy may be used to ensure that learning is outcome- and employability-based.
- Do not let students work on an activity or an experiment with the expected outcome, rather allow students to be honest about whatever the results of the experiment are. If the results are different from the expectations, students should do an analysis where they could be the source of error, if any.



DIRECTORATE OF TECHNICAL EDUCATION, CHENNAI - 600 025

Electrical Circuits and Machines

| L | Т | Ρ | С |
|---|---|---|---|
| 1 | 0 | 2 | 2 |

Practicum

Assessment Methodology

| | C | End Semester | | | |
|-----------------------|---|--|------------------------|-----------------------|--------------------------|
| | CA1 | CA2 | CA3 | CA4 | (60 marks) |
| Mode | Practical Test | Practical Test | Written Test Theory | Practical Test | Practical Examination |
| Portion | Cycle I Experiments/ 50% Experiments | Cycle II Experiments/ Another 50% Experiments | All Units | All Experiments | All Experiments |
| Duration | 2 Periods | 2 Periods | 3 hours | 3 hours | 3 hours |
| Exam Marks | 60 | 60 | 100 | 100 | 100 |
| Converted to | 10 | 10 | 15 | 15 | 60 |
| Marks | 10 | | 15 | 15 | 60 |
| Tentative Schedule | 7 th Week | 14 th Week | 15 th Week | 16 th Week | |

Note:

CA1 and CA2: All the exercises/experiments should be completed as per the portions above and kept for the practical test. The students shall be permitted to select any one by lot for the test. The practical test should be conducted as per the scheme of evaluation as below. The marks awarded shall be converted to 10 Marks for each assessment test. The best one out of two will be considered for the internal assessment of 10 Marks.

Practical documents should be maintained for every experiment immediately after completion of the practice. The practical document should be submitted for the practical test. The same should be evaluated for 10 Marks for each exercise/experiment. The total marks awarded should be converted to 10 Marks for the practical test as per the scheme of evaluation as below.



Practicum

| L | Т | Ρ | С |
|---|---|---|---|
| 1 | 0 | 2 | 2 |

The details of the documents to be prepared as per the instruction below

- The experiment should be completed on the day of practice.
- The same shall be evaluated for 10 marks on the day or next day of practice before commencement of the next experiment.
- This documentation can be carried out in a separate notebook / printed manual / file. The Circuit Diagram, Readings, Calculations and Graph/Result should be written by the student manually.
- The detailed date of the practices and its evaluations should be maintained in the course log book. The log book and the practical documents should be submitted for the verification by the Flying Squad and DOTE Official.

SCHEME OF EVALUATION

| Part | Description | Marks |
|------|-------------------------------------|-------|
| А | Aim | 5 |
| В | Circuit Diagram | 20 |
| С | Connections / Output | 25 |
| D | Practical document (All Practicals) | 10 |
| | 60 | |

CA 3: Written Test for complete theory portions should be conducted for 100 Marks as per the question pattern below. The marks scored will be converted to 15 Marks for internal assessment.

Question pattern – Written Test Theory

| | Description | Marks | | |
|----------|---|--------------|----------|--|
| Part – A | 30 MCQ Questions. | 30 X 1 Mark | 30 Marks | |
| Part – B | 7 Questions to be answered out of 10 Questions. | 7 X 10 Marks | 70 Marks | |



| 1040233640 | Electrical Circuits and | L | Т | Ρ | С |
|------------|-------------------------|---|---|---|---|
| Practicum | Machines | 1 | 0 | 2 | 2 |

CA 4: All the exercises/experiments should be completed and kept for the practical test. The students shall be permitted to select any one by lot for the test. The practical test should be conducted as per the scheme of evaluation below. After completion of all the exercises the practical test should be conducted as per End Semester Examination question pattern scheme of evaluation. The marks awarded should be converted to 15 Marks for the internal assessment.

SCHEME OF EVALUATION

Model Practical Examination and End Semester Examination -Practical Exam

| Part | Description | Marks |
|------|--------------------------|-------|
| А | Aim & Apparatus Required | 5 |
| В | Circuit Diagram | 20 |
| С | Connections / Execution | 25 |
| D | Output / Result | 10 |
| E | Written Test | 30 |
| F | Viva Voce | 10 |
| | TOTAL MARKS | 100 |

Note: For the written test 30 MCQ shall be asked from the theory portions.



| 1040233640 | | Electrical Circuits and | | Т | Ρ | С |
|---|---|--|-----------------------------------|--------|-----|---|
| Practicum | | Machines | 1 | 0 | 2 | 2 |
| Unit I | BASIC ELECTRICAL CIRCUITS | | | | | |
| Ohm's law, Kirchhoff's Current Law, and Kirchhoff's Voltage Law, Equivalent Resistance of Resistors Connected in Series and Parallel- Voltage Division Rule - Current Division Rule for two Branch Parallel Resistive Network - Mesh Analysis and Node Analysis. | | | | | | 3 |
| Ex.No | | Name of the Experiment | | | | |
| 1 | Cons Law | struct a Resistive Network to Verify Kirchhoff's | s Vo | ltage | - 6 | 5 |
| 2 | Cons Law | struct a Resistive Network to Verify Kirchhoff | ′sCu | rrent | | - |
| Unit II | NET | WORK THEOREMS | | | | |
| Thevenin's Transfer T | s The Theore | eorem – Superposition Theorem – Maximur em - Simple Problems. | n P | ower | | 3 |
| Ex.No | | Name of the Experiment | Name of the Experiment | | | |
| 3 | Construct a Resistive Network to Verify the Superposition Theorem. | | | | | 6 |
| 4 | Construct a Resistive Network to Verify Thevenin's Theorem. | | | | | |
| Unit III AC CIRCUITS | | | | | | |
| Sinusoidal AC voltage Characteristics, AC Response of Basic Resistance, Inductance, and Capacitance - Definition for Impedance, Reactance, Admittance and Power Factor. | | | | 3 | | |
| Ex.No | | Name of the Experiment | | | | |
| 5 | Analysis of the sinusoidal waveform (Measurement of Peak Voltage, Time Period, Frequency and Phase difference between two waveforms) | | | | 6 | |
| 6 | and | C. | 033 | i∖, ∟, | | |
| Unit IV RESONANCE IN RLC CIRCUITS | | | | | | |
| Series Resonance Circuit – Parallel Resonance Circuit – Condition for Resonance, Quality Factor (Q), Band Width, Resonance Frequency and Frequency Response Curve. | | | | | 3 | |
| Ex.No | Name of the Experiment | | | | | |
| 7 | Cons | struct and test the performance of Series Resonance | he performance of Series Resonant | | | |
| 8 | Circuit and obtain the Resonance Frequency. Construct and test the performance of parallel resonant circuit and obtain the Resonance frequency. | | | | 6 | |



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| Practicum | | Machines | 1 | 0 | 2 | 2 |
| Unit V | ELE | CTRICAL MACHINES | | | | |
| Working Principle of DC Generator and DC Motor – Transformer - Applications of Transformer-Specifications of Transformer, Single Phase Induction Motor. | | | | | | |
| Ex.No | Name of the Experiment | | | | | |
| 9 | Measure the output voltage in step up / step down Transformer. | | | | | |
| 10 | Case study: Study the performance of Single-Phase Induction Motor | | | | | |
| TOTAL HOURS | | | | | 45 | |

Suggested List of Student Activity

- Presentation/Seminars by students on any recent technological developments based on the course
- Periodic class quizzes conducted on a weekly/fortnightly based on the course
- Micro project that shall be an extension of any practical lab exercise to real-world application

TextBooks

- 1. Robert L. Boylestad, Introductory Circuit Analysis, 13th edition, Pearson Education India, 2015
- 2. B.L. Theraja and A.K. Theraja, A Textbook of Electrical Technology, 4th edition, S. Chand and company Ltd., 2005
- 3. Charles K.Alexander and Mathew N.O.Sadiku, Fundamentals of Electric Circuits, McGraw Hill, 5th edition, 2013

Web link for online simulation

- Home page Analog Signals, Network and Measurement Laboratory (iitkgp.ac.in)
- Example JS Simulator Superposition (iitkgp.ac.in)



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Practicum

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List of Equipment Required for a Batch of 30 Students

| SI.No. | Equipment | Quantity |
|--------|--|----------|
| 1 | Dual Regulated Power Supplies (0 – 30V) | 10 |
| 2 | CRO (30 MHz) | 3 |
| 3 | Function Generator (3 MHz) | 6 |
| 4 | Bread Boards | 15 |
| 5 | Resistors, Capacitors, Inductors - sufficient quantities | 30 |
| 6 | Voltmeter (0-10 V) | 10 |
| 7 | Ammeter (0-10 mA) | 10 |
| 8 | Transformer | 1 |
| 9 | Auto Transformer | 1 |
| 10 | Single-Phase Induction Motor | 1 |

